Claims:

1. An apparatus comprising:

a first processor to execute a first set of instructions;

a second processor to execute a second set of instructions;

a first monitor adapted to determine available performance capability of the first processor while executing the first set of instructions; and

a second monitor communicatively coupled to the first monitor and adapted to determine available performance capability of the second processor while executing the second set of instructions, wherein the apparatus is adapted to execute a third set of instructions on the first processor when the available performance capability of the second processor is less than an acceptable performance level to execute the third set of instructions.

2. The apparatus of claim 1, further comprising memory to store the first, second, and third set of instructions.

3. The apparatus of claim 2, wherein the set of instructions comprise instructions of a program selected from the group consisting of an application program and an operating system program.

4. The apparatus of claim 1, wherein the first monitor is adapted to

determine the available performance capacity based on a current operational voltage potential of the first processor.

5. The apparatus of claim 1, wherein the first monitor is adapted to determine the available performance capacity based on an operational frequency of the first processor.

6. The apparatus of claim 1, wherein the wherein the first monitor is provided, at least in part, by a fourth set of instructions being executed on the first processor.

7. The apparatus of claim 6, wherein the first monitor is provided in part by logic circuitry within the first processor.

8. The apparatus of claim 1, wherein the apparatus is adapted to maintain a database to track an historical average of a processor demand needed to execute the third set of instructions.

9. The apparatus of claim 8, wherein the database includes an average million instructions per second (MIPS) to execute the third set of instructions.

10. The apparatus of claim 1, wherein the acceptable performance level is

defined by a user.

11. The apparatus of claim 1, wherein the apparatus is adapted to increase the available performance capability of the second processor when the available performance capability of the first processor is less than the acceptable performance level to execute the third set of instructions on the first processor.

12. The apparatus of claim 11, wherein the apparatus is adapted to increase the MIPS available on the first processor.

13. The apparatus of claim 11, wherein the apparatus is adapted to increase an operational voltage potential of the first processor.

14. The apparatus of claim 11, wherein the apparatus is adapted to increase an operational frequency of the first processor.

15. A method comprising:

polling a first processor to determine if the first processor has sufficient capacity to execute a first set of instructions when a second processor does not have sufficient capacity to execute the first set of instructions.

16. The method of claim 15, further comprising determining an available capacity of the second processor while the second processor is executing a second set of instructions.

17. The method of claim 16, wherein determining the available capacity of the second processor includes determining an available million instructions per second (MIPS) of the second processor.

18. The method of claim 15, further comprising determining if the capacity of the first processor is sufficient to execute the first set of instructions within a user defined performance level.

19. The method of claim 18, further comprising determining historical average execution requirements for the first set of instructions.

20. The method of claim 18, further comprising increasing the available capacity of the second processor if the capacity of the first processor is not

sufficient to execute the first set of instructions within the user defined performance level.

21. The method of claim 19, further comprising storing the historical average execution requirements in a table.

22. The method of claim 15, further comprising reducing the power consumption of the first processor if the first processor has excess capacity to execute a first set of instructions.

23. The method of claim 22, further comprising reducing the voltage potential of the first processor.

24. An article comprising a storage medium having stored thereon instructions, that, when executed by a computing platform, results in:

polling a first processor to determine if the first processor has sufficient capacity to execute a first set of instructions when a second processor does not have sufficient capacity to execute the first set of instructions.

25. The article of claim 24, wherein the instructions, when executed, further result:

determining if the capacity of the first processor is sufficient to execute the first set of instructions within a user defined performance level.

26. The article of claim 25, wherein the instructions, when executed, further result:

determining historical average execution requirements for the first set of instructions.

27. The article of claim 24, wherein the instructions, when executed, further result:

reducing the power consumption of the first processor if the first processor has excess capacity to execute a first set of instructions.